ADCTRIG PAGE 1

1 ;======================================================================

2 ;

3 ; Author : ADI - Apps

4 ;

5 ; Date : October 2003

6 ;

7 ; File : adctrig.asm

8 ;

9 ; Description : Flash led an initial rate of 100ms

10 ; Pressing INTO triggers single conversion

11 ; The ADC result is written to internal memory

12 ; The delay rate is increased

13 ; The program waits for the next INTO to repeat the

14 ; above sequence

15 ;

16 ;======================================================================

17 ;

18 $MOD842 ; Use ADuC842 predefined Symbols

19

0000 20 FLAG EQU 00H ; Define Bit

0000 21 CHAN EQU 00H

22

---- 23 DSEG

0030 24 ORG 0030H

0028 25 LENGTH EQU 40

0030 26 BUFFER: DS LENGTH

27

---- 28 CSEG ; Defines the following as a segment of code

29

0000 30 ORG 0000H ; Load Code at '0'

31

0000 020057 32 JMP MAIN ; Jump to MAIN

33

34 ;======================================================================

35

0003 36 ORG 0003h ; (INT0 ISR)

0003 F5F0 37 MOV B,A ; Copy A (sets delay)

0005 04 38 INC A ; Increment delay

39

0006 D2DC 40 SETB SCONV ; INITIATE A MAIN ADC SINGLE CONVERSION

41

0008 30DFFD 42 JNB ADCI,$ ; Wait for conversion results

43

44 ; Write ADC Result to memory

000B A6DA 45 MOV @R0,ADCDATAH

000D 08 46 INC R0

000E A6D9 47 MOV @R0,ADCDATAL

0010 08 48 INC R0

49

0011 E5F0 50 MOV A,B ; Restore A (sets delay)

0013 04 51 INC A ; Increment delay

52

0014 32 53 RETI ; Return from Interrupt

54

55 ;======================================================================

56

57

004B 58 ORG 004Bh ; Subroutines

ADCTRIG PAGE 2

59

60 ;------------------------------------------------------------------

61

004B 62 DELAY: ; Delays by 10ms \* A

63 ; 10mSec based on 2.09MHZ

64 ; Core Clock

65 ; i.e. default ADuC842 Clock

66

004B F9 67 MOV R1,A ; Acc holds delay variable (1 clock)

004C 7A1B 68 DLY0: MOV R2,#01Bh ; Set up delay loop0 (2 clocks)

004E 7BFF 69 DLY1: MOV R3,#0FFh ; Set up delay loop1 (2 clocks)

0050 DBFE 70 DJNZ R3,$ ; Dec R3 & Jump here until R3 is 0 (3 clocks)

0052 DAFA 71 DJNZ R2,DLY1 ; Dec R2 & Jump DLY1 until R2 is 0 (3 clocks)

0054 D9F6 72 DJNZ R1,DLY0 ; Dec R1 & Jump DLY0 until R1 is 0 (3 clocks)

0056 22 73 RET ; Return from subroutine

74

75

76 ;======================================================================

77

0057 78 MAIN: ; (main program)

79 ; Configure ADC

0057 75EFAC 80 MOV ADCCON1,#0ACh ; power up ADC

005A 75D800 81 MOV ADCCON2,#CHAN ; select channel to convert

82

005D 7830 83 MOV R0,#BUFFER

005F D288 84 SETB IT0 ; INT0 edge triggered

0061 D2AF 85 SETB EA ; enable inturrupts

0063 D2A8 86 SETB EX0 ; enable INT0

87

88

89

0065 740A 90 MOV A,#010 ; Initialize A -> 10

0067 B2B4 91 BLINK: CPL P3.4 ; blink LED using compliment instruction

0069 114B 92 CALL DELAY ; Jump to subroutine DELAY

006B 80FA 93 JMP BLINK ; If FLAG is still cleared the jump to Blink

94

95 END

96

97

98

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

ADCDATAH . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCDATAL . . . . . . . . . . . . D ADDR 00D9H PREDEFINED

ADCI . . . . . . . . . . . . . . B ADDR 00DFH PREDEFINED

B. . . . . . . . . . . . . . . . D ADDR 00F0H PREDEFINED

BLINK. . . . . . . . . . . . . . C ADDR 0067H

BUFFER . . . . . . . . . . . . . D ADDR 0030H

CHAN . . . . . . . . . . . . . . NUMB 0000H

DELAY. . . . . . . . . . . . . . C ADDR 004BH

DLY0 . . . . . . . . . . . . . . C ADDR 004CH

DLY1 . . . . . . . . . . . . . . C ADDR 004EH

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EX0. . . . . . . . . . . . . . . B ADDR 00A8H PREDEFINED

FLAG . . . . . . . . . . . . . . NUMB 0000H NOT USED

IT0. . . . . . . . . . . . . . . B ADDR 0088H PREDEFINED

LENGTH . . . . . . . . . . . . . NUMB 0028H

MAIN . . . . . . . . . . . . . . C ADDR 0057H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

SCONV. . . . . . . . . . . . . . B ADDR 00DCH PREDEFINED